Version : ***0.1***

TECHNICAL SPECIFICATION

MODEL NO. : PD064VX1

☐Customer's Confirmation

Customer

By

☐PVI's Confirmation

Confirmed By

Prepared By

Date: Feb.02,2005

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TECHNICAL SPECIFICATION

CONTENTS

1.Application

This data sheet applies to a color TFT LCD module, PD064VX1.

PD064VX1 module applies to OA product, computer peripheral , industrial meter , image communication and multi-media.. If you must use in severe reliability environment, please don't extend over PVI's reliability test conditions.

If you use PD064VX1, Prime View advises your systems use PVI's timing controller IC (PVI-2002A) which will generate proper timing signals to control PD064VX1.

2. Features

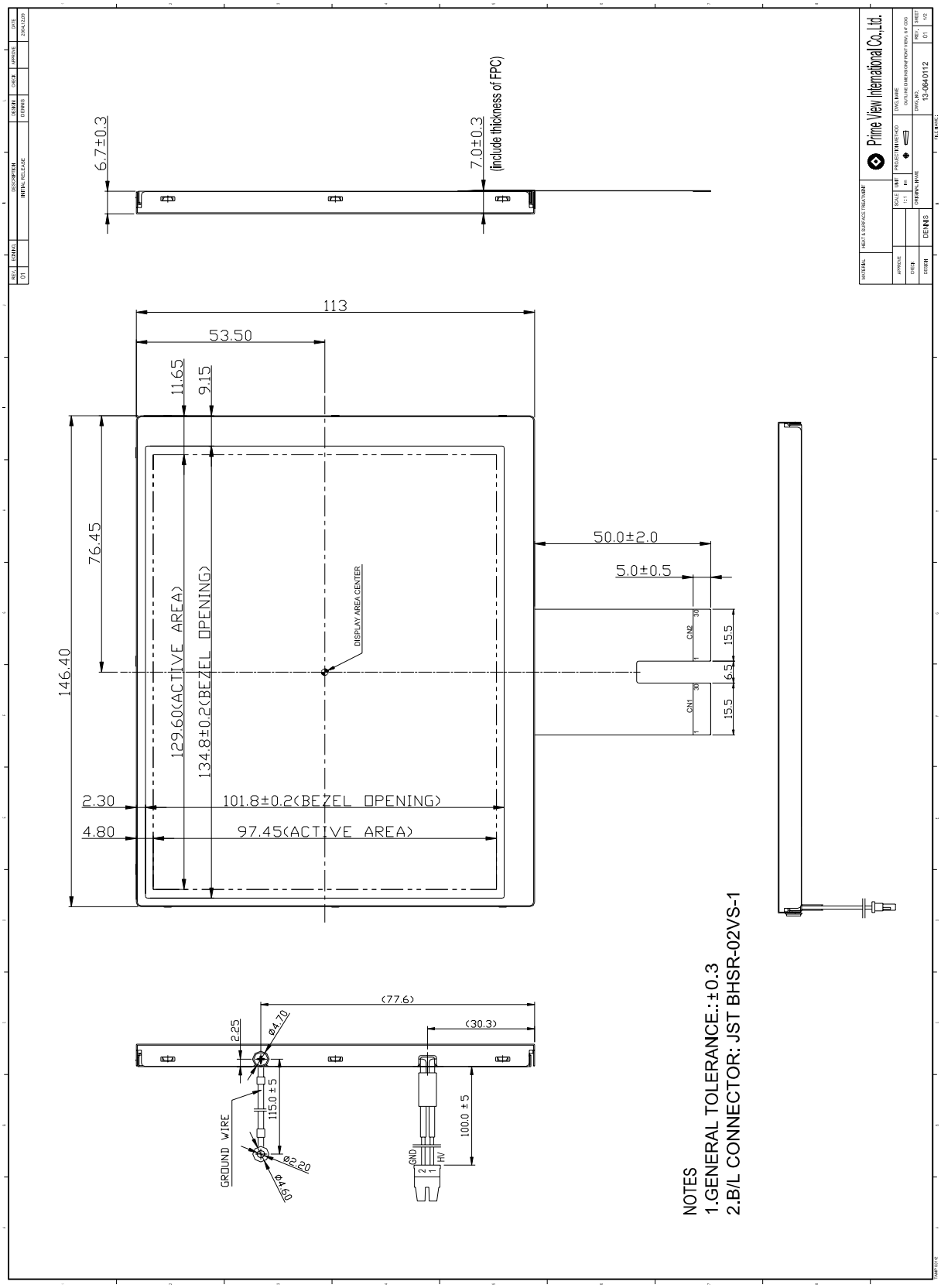
. VGA (640*480 pixels) resolution
. Amorphous silicon TFT LCD panel with back-light unit
. Pixel in stripe configuration
. Thin and light weight
. Display Colors：262,144 colors
. Optimum Viewing Direction：6 o'clock
. TTL transmission interface

3.Mechanical Specifications

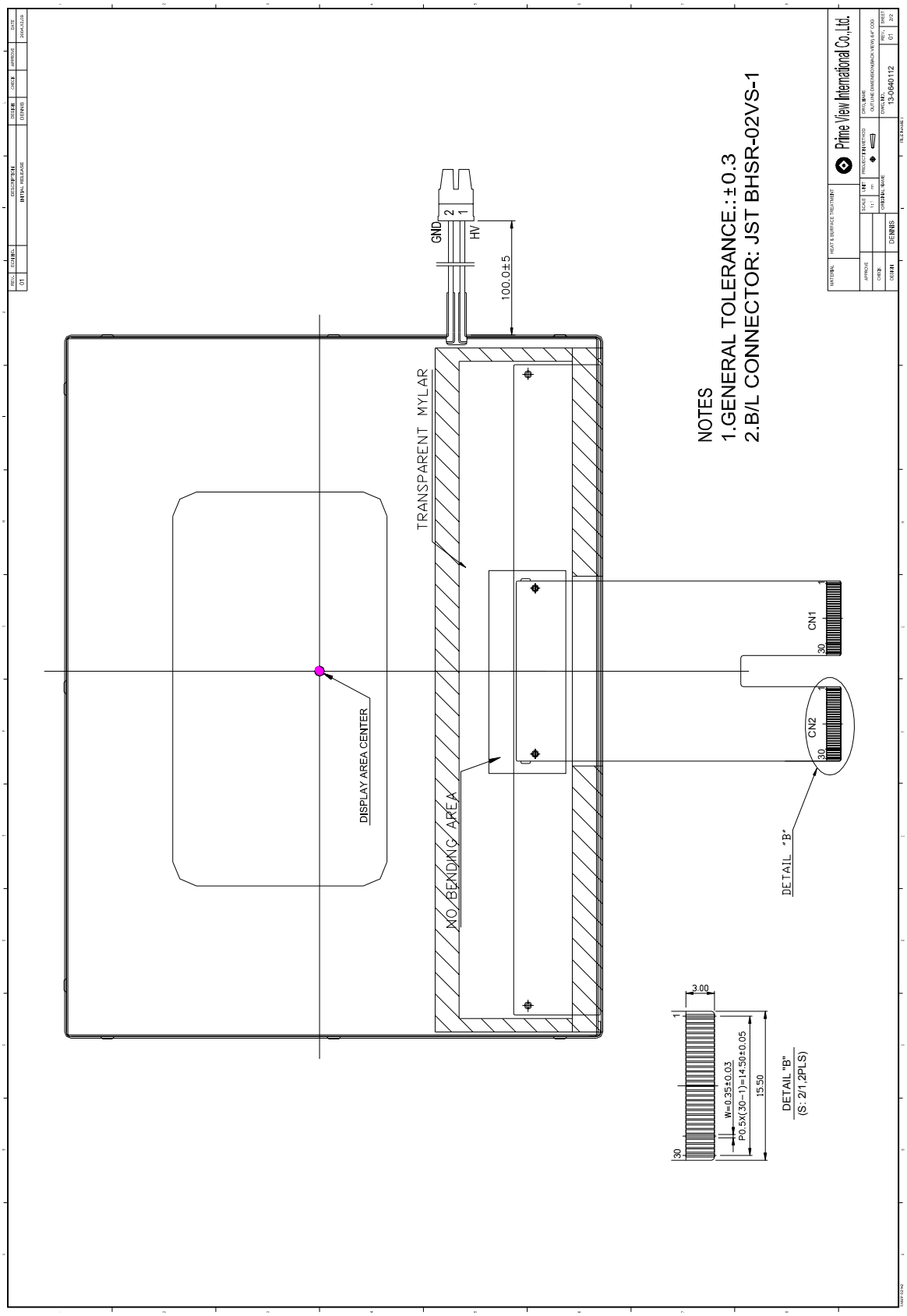
Parameter	Specifications	Unit
Screen Size	6.4(diagonal)	inch
Display Format	640×(R, G, B)×480	dot
Display Colors	262,144	
Active Area	129.6 (H)×97.4 (V)	mm
Pixel Pitch	0.2025 (H)×0.203 (V)	mm
Pixel Configuration	Stripe	
Outline Dimension	146.4(w)×113.0 (H)×6.7 (typ.) (D)	mm
Weight	TBD	g
Back-light	CCFL, 1 tube	
Surface treatment	Anti-glare and hard coating	
Display mode	Normally white	

4.Mechanical Drawing of TFT-LCD Module

Outline Drawing : Front View (unit mm)



Outline Drawing : Rear View (unit mm)



5.Input / Output Terminals

5-1) TFT-LCD Panel Driving

CN 1

Pin No.	Symbol	I/O	Function	Remark
1	DIO1	I/O	Horizontal Start Pulse Signal Input or Output	Note 5-1
2	VSS1	I	Ground	
3	VDD1	I	Power Supply	
4	CLK	I	Horizontal Shift Clock	
5	VSS1	I	Ground	
6	R/L	I	Right / Left selection	Note 5-1
7	R0	I	Red Data (LSB)	
8	R1	I	Red Data	
9	R2	I	Red Data	
10	R3	I	Red Data	
11	R4	I	Red Data	
12	R5	I	Red Data (MSB)	
13	VSS1	I	Ground	
14	G0	I	Green Data (LSB)	
15	G1	I	Green Data	
16	G2	I	Green Data	
17	G3	I	Green Data	
18	G4	I	Green Data	
19	G5	I	Green Data (MSB)	
20	VSS1	I	Ground	
21	B0	I	Blue Data (LSB)	
22	B1	I	Blue Data	
23	B2	I	Blue Data	
24	B3	I	Blue Data	
25	B4	I	Blue Data	
26	B5	I	Blue Data (MSB)	
27	LD	I	Load output signal	Note 5-2
28	REV	I	Data invert control	Note 5-3
29	POL	I	Polarity selection	Note 5-4
30	DIO2	I/O	Horizontal Start Pulse Signal Input or Output	Note 5-1

CN 2

Pin No.	Symbol	I/O	Function	Remark
1	VSS2	I	Ground	
2	V1	I	Gamma Voltage 1	Note 5-10
3	V2	I	Gamma Voltage 2	Note 5-10
4	V3	I	Gamma Voltage 3	Note 5-10
5	V4	I	Gamma Voltage 4	Note 5-10
6	V5	I	Gamma Voltage 5	Note 5-10
7	V6	I	Gamma Voltage 6	Note 5-10
8	V7	I	Gamma Voltage 7	Note 5-10
9	VSS2	I	Ground	
10	V8	I	Gamma Voltage 8	Note 5-10
11	V9	I	Gamma Voltage 9	Note 5-10
12	V10	I	Gamma Voltage 10	Note 5-10
13	V11	I	Gamma Voltage 11	Note 5-10
14	V12	I	Gamma Voltage 12	Note 5-10
15	V13	I	Gamma Voltage 13	Note 5-10
16	V14	I	Gamma Voltage 14	Note 5-10
17	VSS2	I	Ground	
18	VDD2	I	Voltage for analog circuit	Note 5-10
19	VCOM	I	Common Voltage	
20	XON	I	NC	
21	OE	I	Output Enable	Note 5-5
22	U/D	I	Up / Down Selection	Note 5-6
23	CKV	I	Vertical Shift Clock	Note 5-7
24	STVU	I/O	Vertical Shift Pulse Signal Input or Output	Note 5-6
25	STVD	I/O	Vertical Shift Pulse Signal Input or Output	Note 5-6
26	VGG	I	Gate On Voltage	Note 5-8
27	GND	I	Ground	
28	VCC	I	Voltage for logic circuit	
29	GND	I	Ground	
30	VEE	I	Gate Off Voltage	Note 5-9

Note 5-1: Select left or right shift

R/L	DIO1	DIO2	Shift
1	Input	Hi-Z	Left to right
0	Hi-Z	Input	Right to left

Note 5-2: Latch the polarity of outputs and switch the new data to outputs
At the rising edge (LD), latch the “POL” signal to control the polarity of the outputs.

Note 5-3: Control whether the Data R0~G5 are inverted or not. (PVI suggests connecting to GND)
When “REV=1”, these data will be inverted.
EX: “00”→”3F”, “07”→”38”, “15”→”2A”

Note 5-4: Polarity selector for dot-inversion control. Available at the rising edge of LD.
When POL=1: Even outputs range from V1~V7, and Odd outputs range from V8~V14;
When POL=0: Even outputs range from V8~V14, and Odd outputs range from V1~V7.

Note 5-5: When OE is connected to high “1”, the driver outputs are disabled (Gate output = V_{EE}).
Under this condition, the operation of registers will not be affected.

Note 5-6: Select up or down shift

U/D	STVU	STVD	Shift
1	Hi-Z	Input	Down to Up
0	Input	Hi-Z	Up to Down

Note 5-7: Gate driver shift clock

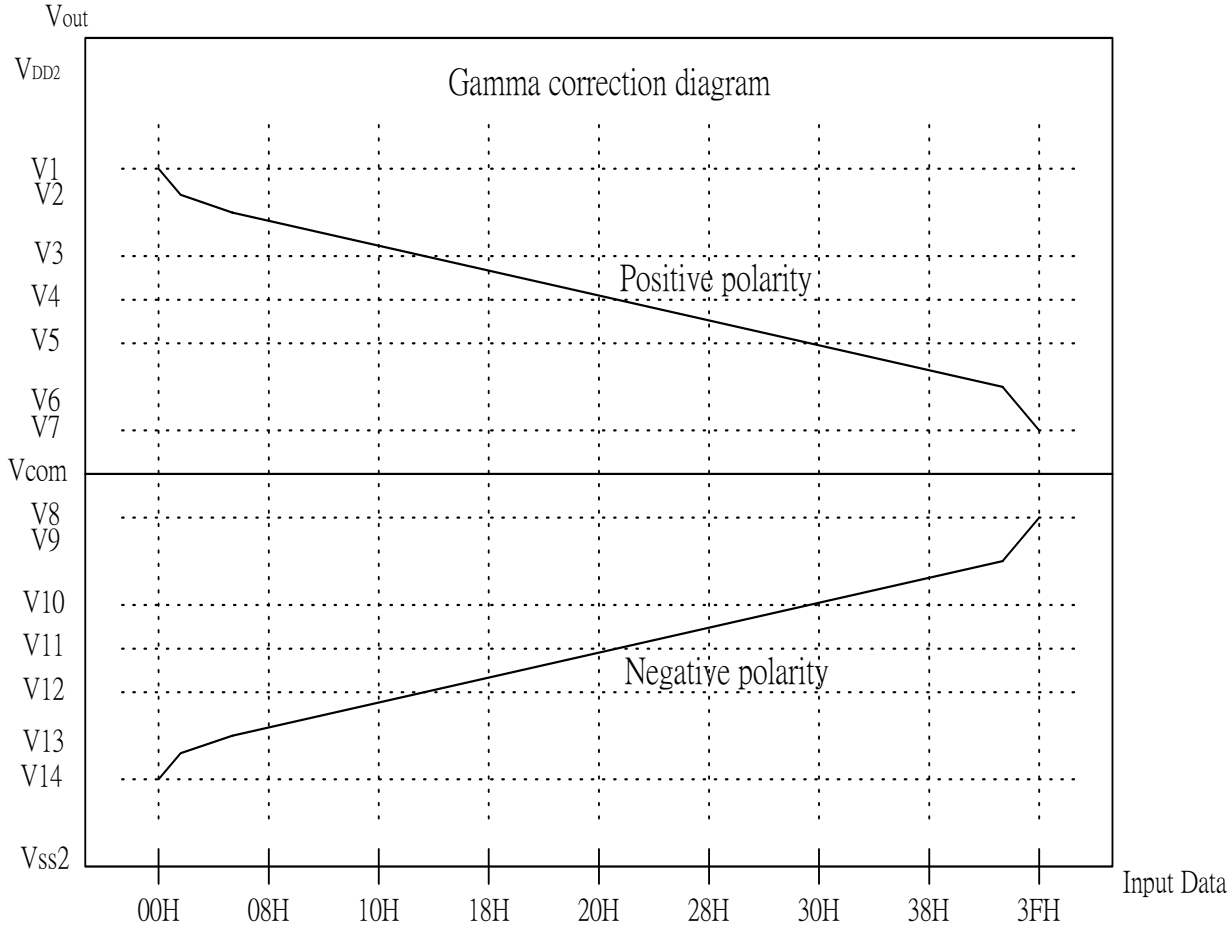
Note 5-8: Gate on voltage, V_{GG}=TBD

Note 5-9: Gate off voltage, V_{EE}=TBD

Note 5-10:

1) Relationship between input data and output voltage

The figure below shows the relationship between the input data and the output voltage to panel with the polarity. The range of V1~V7 is for positive polarity, and V8~V14 for negative polarity. Please refer to the following pages to get the related resister values and voltage calculation method.



Remark: V_{DD2}-0.1≧V1≧V2≧V3≧V4≧V5≧V6≧V7; V8≧V9≧V10≧V11≧V12≧V13≧V14≧ V_{SS2}+0.1V.

2) Output voltage and input data
Output Voltage to Panel VS Input Data

Data	Positive polarity Output Voltage	Negative polarity Output Voltage
00H	V1	V14
01H	V2=V3+(V1-V3) × 58 / 64.4	V13=V14+(V12-V14) × 6.4 / 64.4
02H	V3+(V1-V3) × 52 / 64.4	V14+(V12-V14) × 12.4 / 64.4
03H	V3+(V1-V3) × 46.4 / 64.4	V14+(V12-V14) × 18 / 64.4
04H	V3+(V1-V3) × 41.2 / 64.4	V14+(V12-V14) × 23.2 / 64.4
05H	V3+(V1-V3) × 36.4 / 64.4	V14+(V12-V14) × 28 / 64.4
06H	V3+(V1-V3) × 32 / 64.4	V14+(V12-V14) × 32.4 / 64.4
07H	V3+(V1-V3) × 27.6 / 64.4	V14+(V12-V14) × 36.8 / 64.4
08H	V3+(V1-V3) × 23.6 / 64.4	V14+(V12-V14) × 40.8 / 64.4
09H	V3+(V1-V3) × 19.6 / 64.4	V14+(V12-V14) × 44.8 / 64.4
0AH	V3+(V1-V3) × 16.4 / 64.4	V14+(V12-V14) × 48 / 64.4
0BH	V3+(V1-V3) × 13.2 / 64.4	V14+(V12-V14) × 51.2 / 64.4
0CH	V3+(V1-V3) × 10.4 / 64.4	V14+(V12-V14) × 54 / 64.4
0DH	V3+(V1-V3) × 7.6 / 64.4	V14+(V12-V14) × 56.8 / 64.4
0EH	V3+(V1-V3) × 4.8 / 64.4	V14+(V12-V14) × 59.6 / 64.4
0FH	V3+(V1-V3) × 2.4 / 64.4	V14+(V12-V14) × 62 / 64.4
10H	V3	V12
11H	V4+(V3-V4) × 19.6 / 22	V12+(V11-V12) × 2.4 / 22
12H	V4+(V3-V4) × 17.6 / 22	V12+(V11-V12) × 4.4 / 22
13H	V4+(V3-V4) × 15.6 / 22	V12+(V11-V12) × 6.4 / 22
14H	V4+(V3-V4) × 13.6 / 22	V12+(V11-V12) × 8.4 / 22
15H	V4+(V3-V4) × 12 / 22	V12+(V11-V12) × 10 / 22
16H	V4+(V3-V4) × 10.4 / 22	V12+(V11-V12) × 11.6 / 22
17H	V4+(V3-V4) × 8.8 / 22	V12+(V11-V12) × 13.2 / 22
18H	V4+(V3-V4) × 7.6 / 22	V12+(V11-V12) × 14.4 / 22
19H	V4+(V3-V4) × 6.4 / 22	V12+(V11-V12) × 15.6 / 22
1AH	V4+(V3-V4) × 5.2 / 22	V12+(V11-V12) × 16.8 / 22
1BH	V4+(V3-V4) × 4 / 22	V12+(V11-V12) × 18 / 22
1CH	V4+(V3-V4) × 3.2 / 22	V12+(V11-V12) × 18.8 / 22
1DH	V4+(V3-V4) × 2.4 / 22	V12+(V11-V12) × 19.6 / 22
1EH	V4+(V3-V4) × 1.6 / 22	V12+(V11-V12) × 20.4 / 22
1FH	V4+(V3-V4) × 0.8 / 22	V12+(V11-V12) × 21.2 / 22

Output Voltage to Panel VS Input Data(continued)

Data	Positive polarity Output Voltage	Negative polarity Output Voltage
20H	V4	V11
21H	V5+(V4-V5) × 12 / 12.8	V11+(V10-V11) × 0.8 / 12.8
22H	V5+(V4-V5) × 11.2 / 12.8	V11+(V10-V11) × 1.6 / 12.8
23H	V5+(V4-V5) × 10.4 / 12.8	V11+(V10-V11) × 2.4 / 12.8
24H	V5+(V4-V5) × 9.6 / 12.8	V11+(V10-V11) × 3.2 / 12.8
25H	V5+(V4-V5) × 8.8 / 12.8	V11+(V10-V11) × 4 / 12.8
26H	V5+(V4-V5) × 8 / 12.8	V11+(V10-V11) × 4.8 / 12.8
27H	V5+(V4-V5) × 7.2 / 12.8	V11+(V10-V11) × 5.6 / 12.8
28H	V5+(V4-V5) × 6.4 / 12.8	V11+(V10-V11) × 6.4 / 12.8
29H	V5+(V4-V5) × 5.6 / 12.8	V11+(V10-V11) × 7.2 / 12.8
2AH	V5+(V4-V5) × 4.8 / 12.8	V11+(V10-V11) × 8 / 12.8
2BH	V5+(V4-V5) × 4 / 12.8	V11+(V10-V11) × 8.8 / 12.8
2CH	V5+(V4-V5) × 3.2 / 12.8	V11+(V10-V11) × 9.6 / 12.8
2DH	V5+(V4-V5) × 2.4 / 12.8	V11+(V10-V11) × 10.4 / 12.8
2EH	V5+(V4-V5) × 1.6 / 12.8	V11+(V10-V11) × 11.2 / 12.8
2FH	V5+(V4-V5) × 0.8 / 12.8	V11+(V10-V11) × 12 / 12.8
30H	V5	V10
31H	V7+(V5-V7) × 26.8 / 27.6	V10+(V8-V10) × 0.8 / 27.6
32H	V7+(V5-V7) × 26 / 27.6	V10+(V8-V10) × 1.6 / 27.6
33H	V7+(V5-V7) × 25.2 / 27.6	V10+(V8-V10) × 2.4 / 27.6
34H	V7+(V5-V7) × 24.4 / 27.6	V10+(V8-V10) × 3.2 / 27.6
35H	V7+(V5-V7) × 23.6 / 27.6	V10+(V8-V10) × 4 / 27.6
36H	V7+(V5-V7) × 22.4 / 27.6	V10+(V8-V10) × 5.2 / 27.6
37H	V7+(V5-V7) × 21.2 / 27.6	V10+(V8-V10) × 6.4 / 27.6
38H	V7+(V5-V7) × 20 / 27.6	V10+(V8-V10) × 7.6 / 27.6
39H	V7+(V5-V7) × 18.4 / 27.6	V10+(V8-V10) × 9.2 / 27.6
3AH	V7+(V5-V7) × 16.8 / 27.6	V10+(V8-V10) × 10.8 / 27.6
3BH	V7+(V5-V7) × 14.8 / 27.6	V10+(V8-V10) × 12.8 / 27.6
3CH	V7+(V5-V7) × 12.8 / 27.6	V10+(V8-V10) × 14.8 / 27.6
3DH	V7+(V5-V7) × 10.4 / 27.6	V10+(V8-V10) × 17.2 / 27.6
3EH	V7+(V5-V7) × 6.4 / 27.6	V10+(V8-V10) × 21.2 / 27.6
3FH	V7	V8

3) Typical Application Circuit (When V_{DD2} = +9.5V)
TBD

5-2) Backlight driving

Connector type: JST BHR-03VS-1 , Pin No. : 3 , Pitch : 4 mm

Pin No	Symbol	Description	Remark
1	VL1	Input terminal (Hi voltage side)	Wire color : Pink
2	VL2	Input terminal (Low voltage side)	Wire Color : White Note 5-2

Note 5-2 : Low voltage side of backlight inverter connects with ground of inverter circuits.

6.Absolute Maximum Ratings:

$V_{SS1}=V_{SS2}=GND=0V$, Ta=25℃

Parameters	Symbol	MIN.	MAX.	Unit	Remark
Supply Voltage	V_{DD1}	-0.3	5.0	V	
	V_{CC}			V	
	V_{DD2}	-0.5	10	V	
	V_{GG}	-0.3	40.0	V	
	V_{GG}-V_{EE}	-	40	V	
	V_{EE}	-20	0.3	V	
Digital Input	V_{IN}	-0.5	V_{CC}+0.5	V	
Backlight Driving Voltage	V_L	-	2000	V	
Backlight Driving Frequency	F_L	0	100	KHz	
Storage Temperature	T_{ST}	TBD	70	℃	
Operating Temperature	T_{OP}	TBD	60	℃	

7.Electrical Characteristics

7-1) Recommended Operating Conditions:

$V_{SS1}=V_{SS2}=GND=0V$, Ta=25℃

Item	Symbol	Min.	Typ.	Max.	Unit	Remark
Supply Voltage for Source Driver	V_{DD1}	3.0	3.3	3.6	V	
	V_{DD2}	9	9.5	10	V	
Supply Voltage for Gate Driver	V_{GG}	-	17	-	V	
	V_{EE}	-	-10	-	V	
	V_{CC}	3.0	3.3	3.6	V	
Digital Input Voltage	V_{IH}	$0.8V_{DD1}$	-	V_{DD1}	V	
	V_{IL}	0	-	$0.2V_{DD1}$	V	

7-2) Recommended Driving Condition for Back Light

Ta=25℃

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
Lamp Voltage	V_L		560	616	V	I_L=6mA
Lamp Current	I_L	5.5	6	6.5	mA	Note 7-1
Lamp Frequency	P_L	35	40	45	KHz	Note 7-2
Starting Voltage (25℃) (Reference Value)	Vs			858	Vrms	Note 7-3
Starting Voltage (0℃) (Reference Value)	Vs			TBD	Vrms	Note 7-3

Note 7-1: In order to satisfy the quality of B/L, no matter use what kind of inverter, the output lamp current must between Min. and Max. to avoid the abnormal display image caused by B/L.

Note 7-2: The waveform of lamp driving voltage should be as closed to a perfect sine wave as possible.

Note 7-3: 1. This value is not output voltage of inverter.
2. The voltage of inverter must larger than the starting voltage.
3. The Kick-off times $\geqq$ 1sec

7-3) Power Consumption

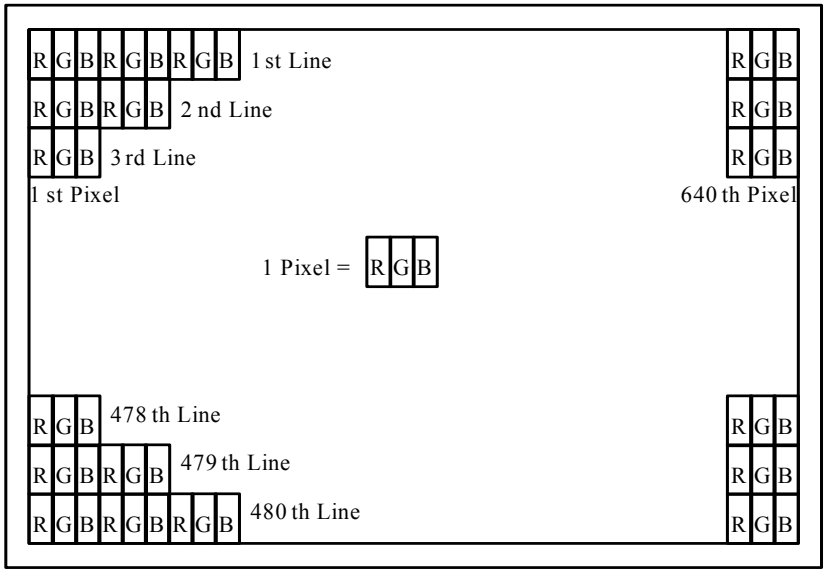
Parameter	Symbol	Condition	Typ.	Max.	Unit	Remark
Supply Current for Gate Driver (Hi level)	I_{GG}	V_{GG}=+17V	TBD	TBD	mA	
Supply Current for Gate Driver (Low level)	I_{EE}	V_{EE}=-10V	TBD	TBD	mA	
Supply Current for Source Driver (Digital)	I_{DD1}	V_{DD1}=+3.3V	TBD	TBD	mA	
Supply Current for Source Driver (Analog)	I_{DD2}	V_{DD2}=+9.5V	TBD	TBD	mA	
Supply Current for Gate Driver (Digital)	I_{CC}	V_{CC}=+3.3V	TBD	TBD	mA	
LCD Panel Power Consumption			TBD	TBD	mW	Note 7-4
Back Light Lamp Power Consumption			TBD		W	Note 7-5

Note 7-4: The power consumption for back light is not included.

Note 7-5: Back light lamp power consumption is calculated by $I_L \times V_L$.

8. Pixel Arrangement

The LCD module pixel arrangement is the stripe.

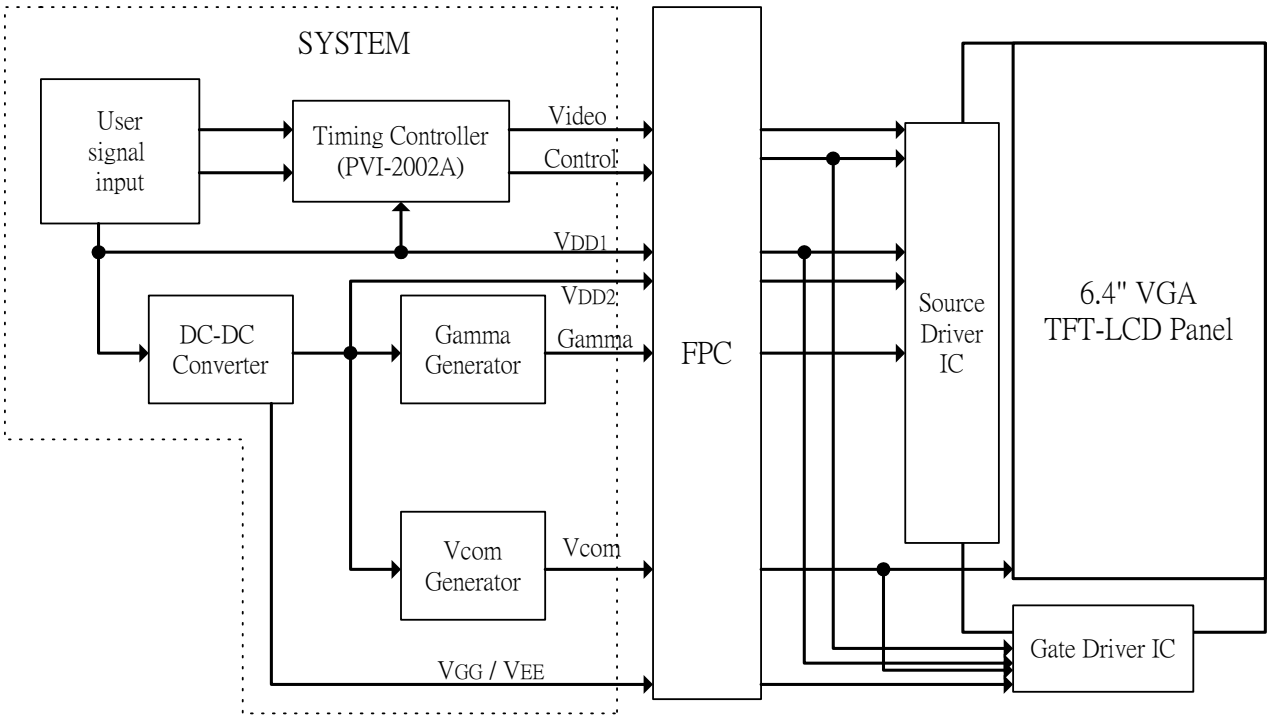


9. Display Color and Gray Scale Reference

Color		Input Color Data																	
		Red						Green						Blue					
		R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (63)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Green (63)	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
	Blue (63)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Red	Red (00)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (01)	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red (02)	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	Darker																		
	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
	Brighter																		
	Red (61)	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red (62)	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (63)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
Green	Green (00)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green (01)	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
	Green (02)	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
	Darker																		
	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
	Brighter																		
	Green (61)	0	0	0	0	0	0	1	1	1	1	0	1	0	0	0	0	0	0
	Green (62)	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0
	Green (63)	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
Blue	Blue (00)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue (01)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue (02)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	Darker																		
	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
	Brighter																		
	Blue (61)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	1
	Blue (62)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0
	Blue (63)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1

10. Block Diagram

10-1) TFT-module Block Diagram



If you use PD064VX1, you can apply PVI-2002A(Timing controller) which will gernerate timing signals to support PD064VX1.

11. Interface Timing

11.1) Timing Parameters

AC Electrical Characteristics (V_{CC}=V_{DD1}=3.3V, V_{DD2}=9.5V, GND=V_{SS1}=V_{SS2}=0V, Ta=25℃)

Parameter	Symbol	Min.	Typ.	Max.	Unit
CLK Frequency	Fclk	-	25	40	MHz
CLK Pulse Width	Tcw	40	-	-	ns
Data Set-up Time	Tsu	4	-	-	ns
Data Hold Time	Thd	2	-	-	ns
Propagation Delay of DIO2/1	Tphl	6	10	15	ns
Time That The Last Data to LD	Tld	1	-	-	Tcw
Pulse width of LD	Twld	2	-	-	Tcw
Time That LD to DIO1/2	Tlds	5	-	-	Tcw
POL Set-up Time	Tpsu	6	-	-	ns
POL Hold Time	Tphd	6	-	-	ns
OE Pulse Width	T_{OEV}	1	-	-	μs
CKV Pulse Width	T_{CKV}	500	-	-	ns
STV Set-up Time	T_{SUV}	400	-	-	ns
STV Hold Time	T_{HDV}	400	-	-	ns
Horizontal Display Period	T_{HDP}	-	640	-	Tcw
Horizontal Period Timing Range	T_{HP}	-	800	-	Tcw
Horizontal Lines Per Field	T_V	TBD	525	TBD	T_{HP}
Vertical Display Timing Range	T_{DV}	-	480	-	T_{HP}

11.2) Timing Diagram

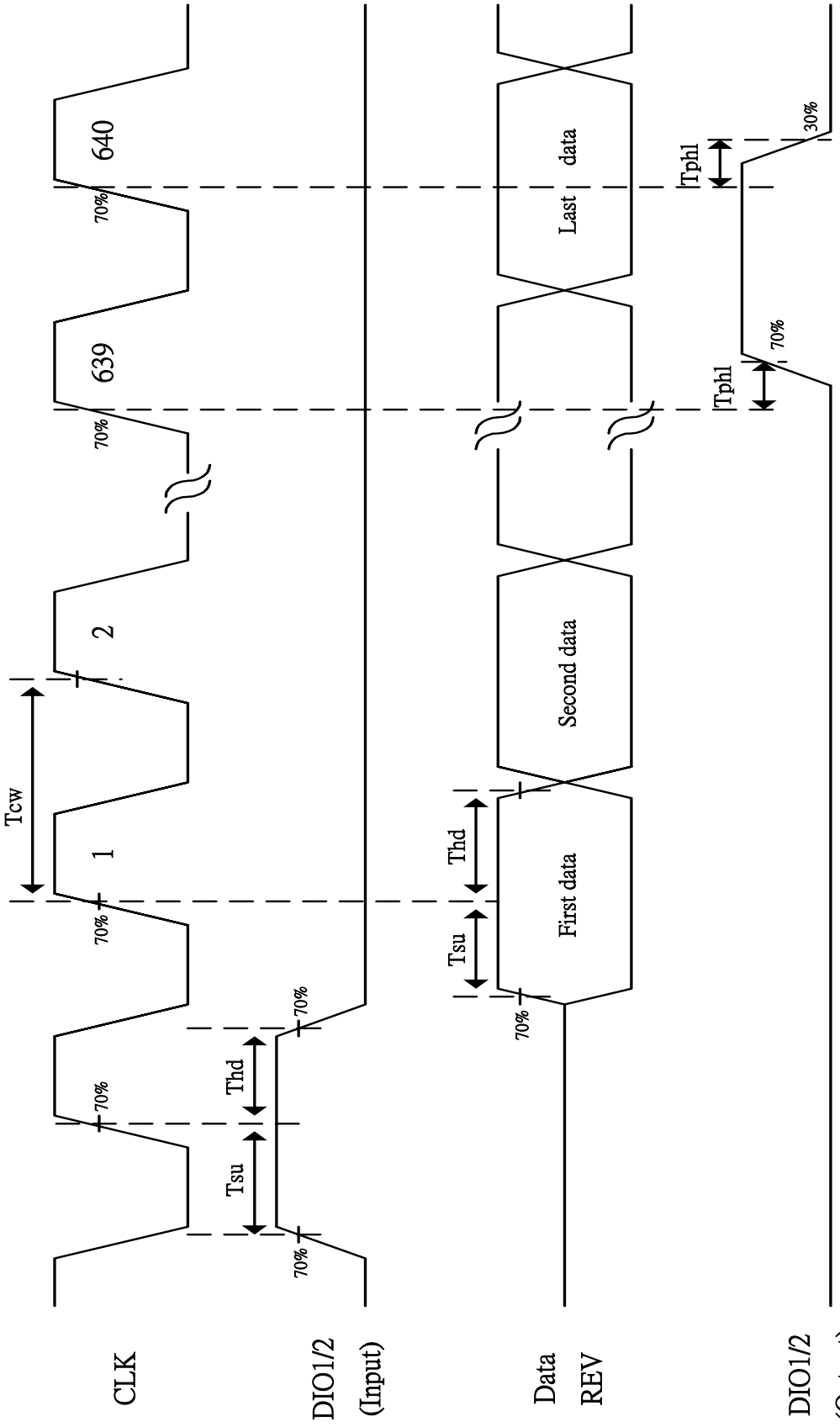


Fig. 11-1 Horizontal timing (1)

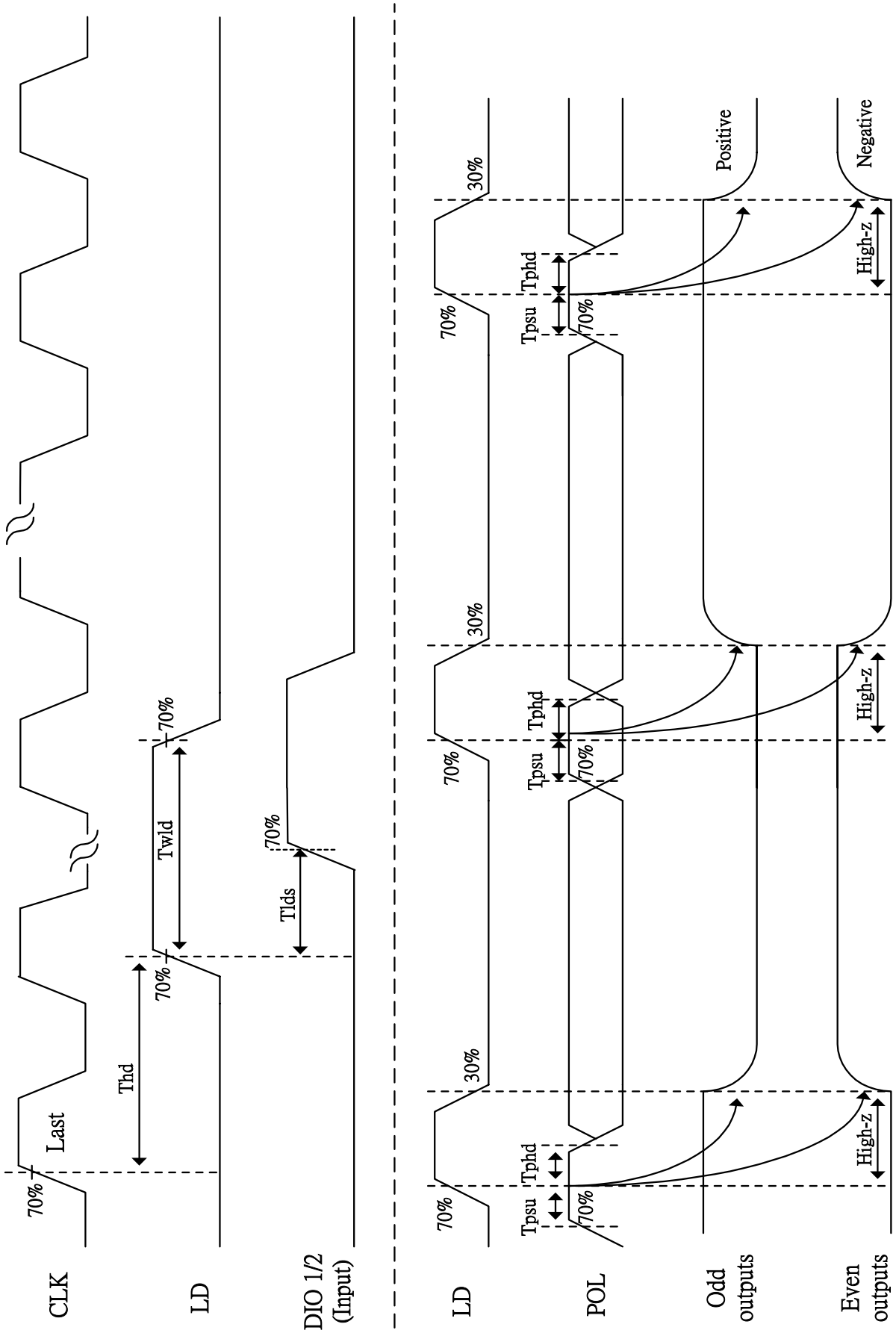


Fig. 11-2 Horizontal timing(2)

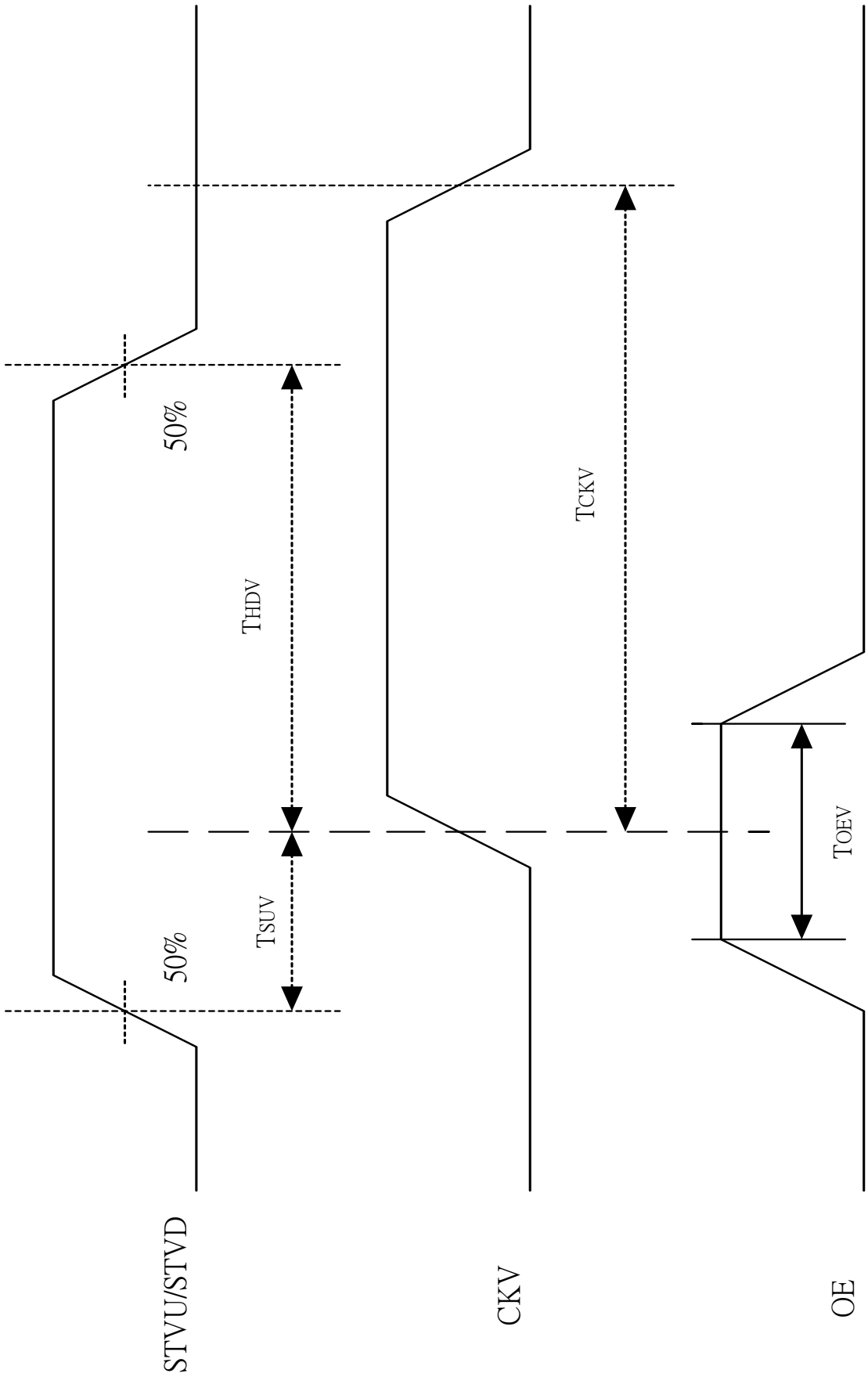


Fig. 11-3 Vertical shift clock timing

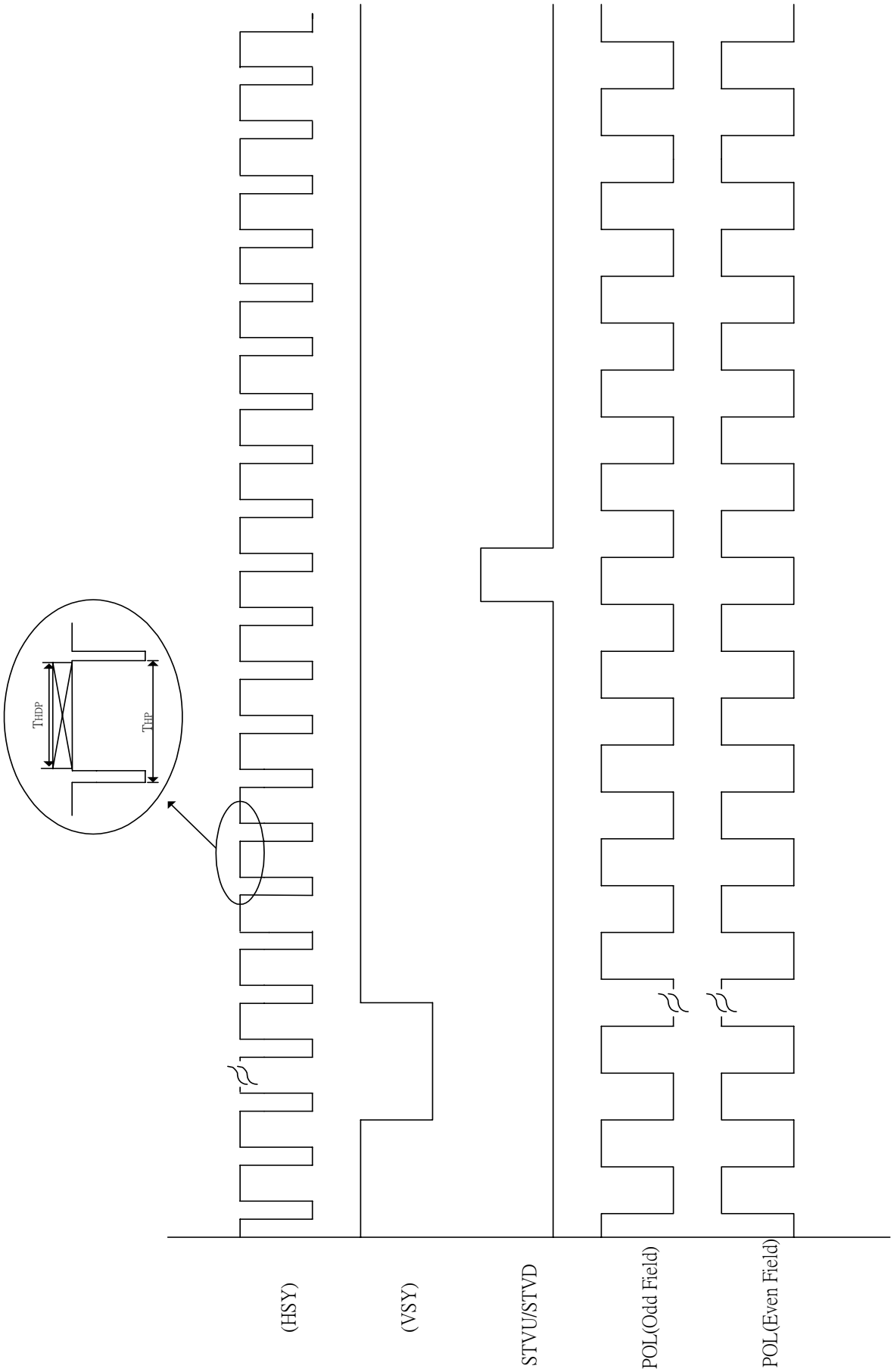
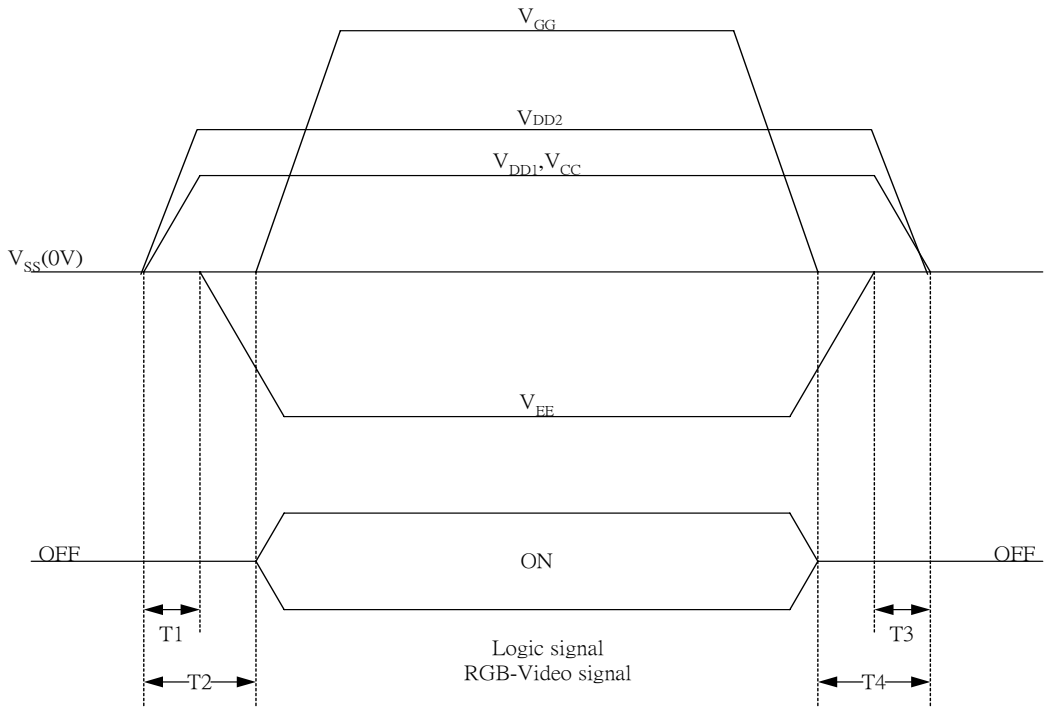


Fig. 11-4 Vertical timing

12. Power On Sequence



1.10ms≦T1＜T2

2. 0ms＜T3≦T4≦10ms

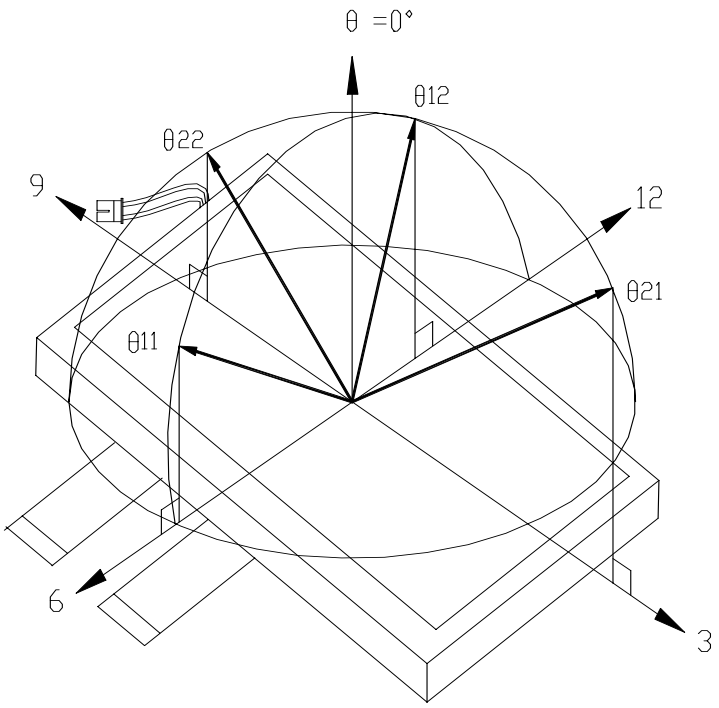
13. Optical Characteristics

13-1) Specification:

Ta=25℃

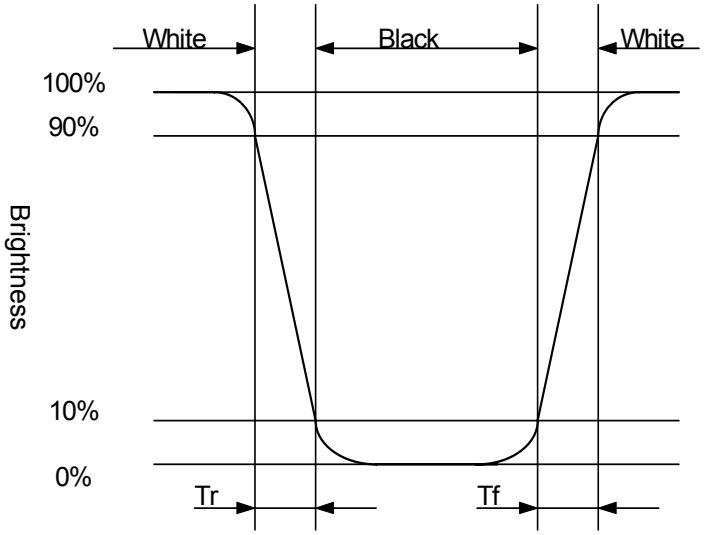
Parameter		Symbol	Condition	MIN.	TYP.	MAX.	Unit	Remarks
Viewing Angle	Horizontal	θ	CR＞10	±45	±50		deg	Note 13-1
	Vertical	θ (to 12 o'clock)		10	15	-	deg	
		θ (to 6 o'clock)		30	35	-	deg	
Contrast Ratio		CR		200	400	-	-	Note 13-2
Response time	Rise	Tr	θ =0°	-	15	30	ms	Note 13-3
	Fall	Tf		-	25	50	ms	
Brightness			θ =0°/ φ =0	TBD	TBD		cd/㎡	Note 13-4
Luminance Uniformity		U		TBD	TBD	-	%	Note 13-5
Lamp Life Time				TBD	-	-	hr	At 6mA
White Chromaticity		x		0.264	0.294	0.325	-	
		y		0.278	0.308	0.338	-	
Cross Talk			θ =0°	-	-	3.5	%	Note 13-6

Note 13-1: The definitions of viewing angles are as follow

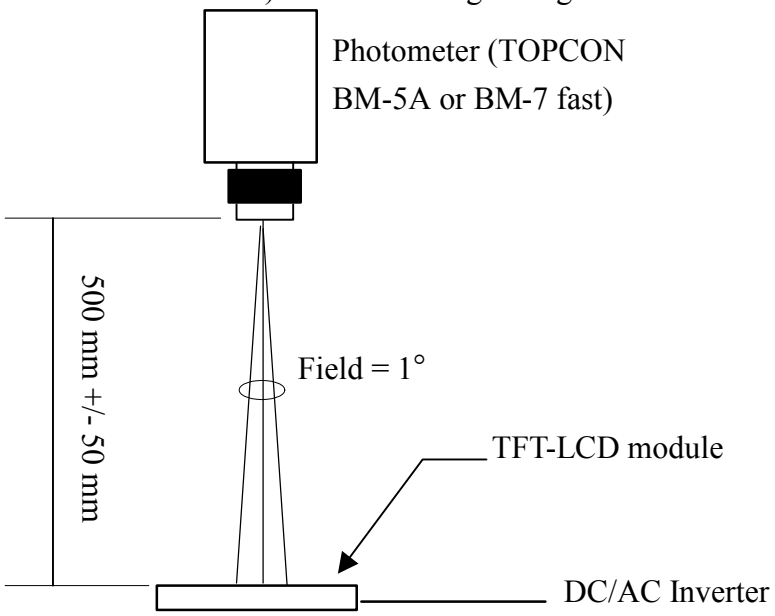


Note 13-2: The definition of contrast ratio $CR = \frac{\text{Luminance at gray level 63}}{\text{Luminance at gray level 0}}$

Note 13-3: Definition of Response Time T_r and T_f:



Note 13-4: All the optical measurement shall be executed 30 minutes after backlight being turn-on. The optical characteristics shall be measured in dark room (ambient illumination on panel surface less than 1 Lux). The measuring configuration shows as following figure.



Optical characteristics measuring configuration

Note 13-5: The uniformity of LCD is defined as

$$U = \frac{\text{The Minimum Brightness of the 9 testing Points}}{\text{The Maximum Brightness of the 9 testing Points}}$$

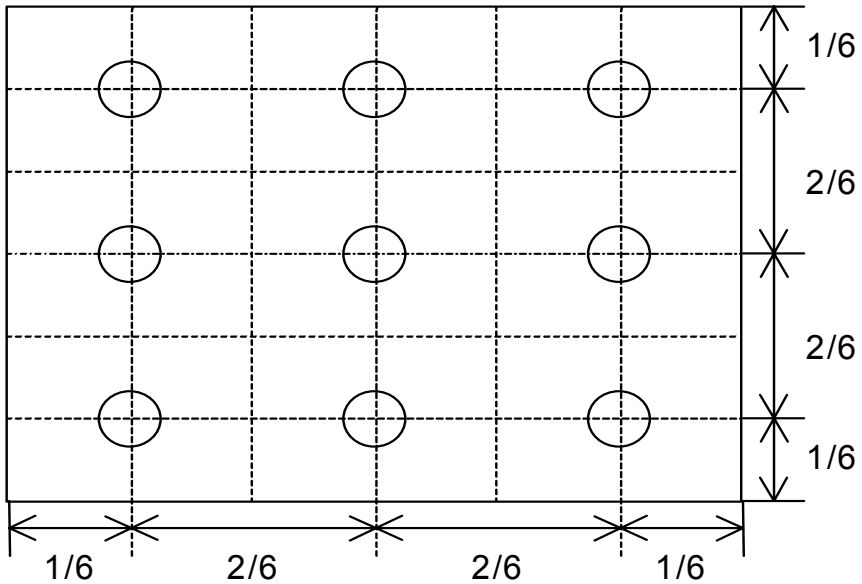
Luminance meter : BM-5A or BM-7 fast(TOPCON)

Measurement distance : 500 mm +/- 50 mm

Ambient illumination : < 1 Lux

Measuring direction : Perpendicular to the surface of module

The test pattern is white (Gray Level 63).



Note 13-6: Cross Talk (CTK) = $\frac{|YA-YB|}{YA} \times 100\%$

YA: Brightness of Pattern A

YB: Brightness of Pattern B

Luminance meter : BM 5A or BM-7 fast (TOPCON)

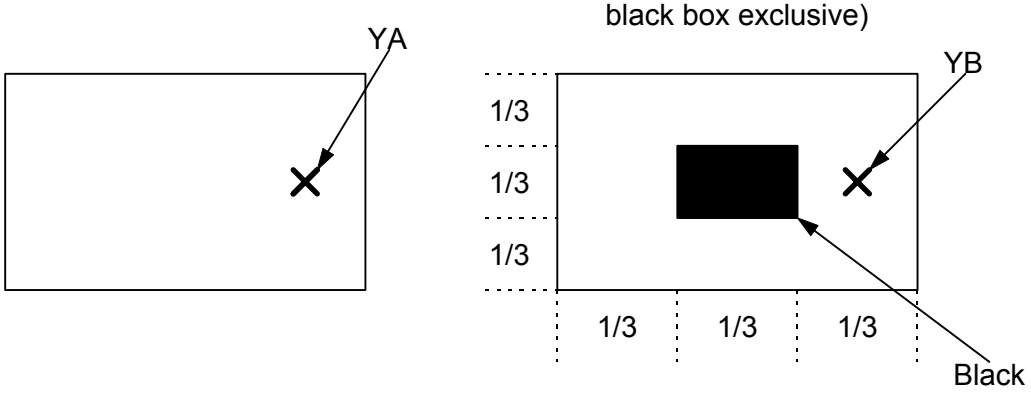
Measurement distance : 500 mm +/- 50 mm

Ambient illumination : < 1 Lux

Measuring direction : Perpendicular to the surface of module

Pattern A
(Gray Level 31)

Pattern B
(Gray Level 31, central
black box exclusive)



✕: Measuring Point (A and B are at the same point.)

(Gray Level 0)

Note 13-7: Topcon BM-5A or BM-7 fast luminance meter 1°field of view is used in the testing (after 30 minutes' operation). The typical luminance value is measured at lamp current 6.0 mA.

14. Handling Cautions

14-1) Mounting of module

a) Please power off the module when you connect the input/output connector.
b) Please connect the ground pattern of the inverter circuit surely. If the connection is not perfect, some following problems may happen possibly.
   1.The noise from the backlight unit will increase.
   2.The output from inverter circuit will be unstable.
   3.In some cases a part of module will heat.
c) Polarizer which is made of soft material and susceptible to flaw must be handled carefully.
d) Protective film (Laminator) is applied on surface to protect it against scratches and dirts. It is recommended to peel off the laminator before use and taking care of static electricity.

14-2) Precautions in mounting

a) When metal part of the TFT-LCD module (shielding lid and rear case) is soiled, wipe it with soft dry cloth.
b) Wipe off water drops or finger grease immediately. Long contact with water may cause discoloration or spots.
c) TFT-LCD module uses glass which breaks or cracks easily if dropped or bumped on hard surface. Please handle with care.
d) Since CMOS LSI is used in the module. So take care of static electricity and earth yourself when handling.

14-3) Adjusting module

a) Adjusting volumes on the rear face of the module have been set optimally before shipment.
b) Therefore, do not change any adjusted values. If adjusted values are changed, the specifications described may not be satisfied.

14-4) Others

a) Do not expose the module to direct sunlight or intensive ultraviolet rays for many hours.
b) Store the module at a room temperature place.
c) The voltage of beginning electric discharge may over the normal voltage because of leakage current from approach conductor by to draw lump read lead line around.
d) If LCD panel breaks, it is possibly that the liquid crystal escapes from the panel. Avoid putting it into eyes or mouth. When liquid crystal sticks on hands, clothes or feet. Wash it out immediately with soap.
e) Observe all other precautionary requirements in handling general electronic components.
f) Please adjust the voltage of common electrode as material of attachment by 1 module.

15. Reliability Test

No	Test Item	Test Condition	Remark
1	High Temperature Storage Test	Ta = +70℃, 240 hrs	
2	Low Temperature Storage Test	TBD	
3	Low Temperature Operation Test	TBD	
4	High Temperature & High Humidity Operation Test	Ta = +60℃, 90%RH, 240 hrs (No Condensation)	
5	Thermal Cycling Test (non-operating)	-20℃→+70℃, 200 Cycles 30min 30min	
6	Vibration Test (non-operating)	Frequency : 10 ~ 57 H_Z /Vibration Width :0.075mm 58-500 H/ / Gravity :9.8m/s Sweep time: 11 minutes Test period: 3 hrs for each direction of X, Y, Z	
7	Shock Test (non-operating)	Gravity :490m/s Direction: ±X, ±Y, ±Z Pulse Width :11ms,half sine wave	
8	Electrostatic Discharge Test (non-operating)	150pF, 330Ω Air : ±15KV ; Contact : ±8KV 10 times/point , 9 points/panel face	

Ta: ambient temperature

Note 15-1 : The protective film must be removed before temperature test.

[Judgement Criteria]

Under the display quality test conditions with normal operation state , there should be no change which may affect practical display function.

16. Packing Diagram

TBD

Revision History

Rev.	Issued Date	Revised Contents
0.1	Feb.02, 2005	New